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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,208	MCCOWN, HAL C.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 were examined.

Substitute Specification, Drawings and Claims

2. The Office has accepted the substitute specification, drawings and claims.

Claim Objections

3. Claims 15-20 are objected to because of the following informalities: "computer readable memory" is unclear as to how memory directs a computer. The Office suggests amending the claims with "computer readable medium with "instructions" so the record is clear.

4. Claim 9 is objected to since the limitations reflect an apparatus type claim, which is linked to a method claim, thus integrating different statutory types.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103 (a) as obvious by Dearth (US Patent 5,907,695) in view of Beausang et al., (US Patent 5,696,771) (hereafter Beausang) and in further view of Sharma et al., (US Patent 5,841,663) (hereafter Sharma). Dearth, Beausang and Sharma are analogous art because all teach HDL simulation of circuits.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the behavioral relationships in Dearth, and the timing violations of Beausang in the parameterization of Sharma because Dearth teaches a convenient and efficient division of a simulation of circuit (Dearth: column 21, lines 28-30); and Beausang teaches a set of sequential cells that can be scan replaced to just meet the timing and area constraints while offering significant testability for the design (Beausang: column 4, lines 22-25).

Claim 1. An integrated circuit ("IC") simulation system operable to (i) store a plurality of Hardware Description Language ("HDL") modules (Sharma: title), each one of said plurality of HDL modules (Sharma: title) representative of a circuit element, (ii) receive a HDL description of a circuit to be simulated (Sharma: column 1, line 19), and (iii) synthesize a circuit netlist (Sharma: column 1, line 24 and column 35, line 51) as a

function of said received HDL circuit description and ones of said plurality of HDL modules (Sharma: title), said circuit netlist (Sharma: column 1, line 24) defining behavioral relationships (Dearth: column 1, lines 58-60) among associated ones of said ones of said plurality of HDL modules (Sharma: title), and associate a timing-violation controller with said circuit netlist (Sharma: column 1, line 24), said timing-violation controller to ignore selected timing violations sensed (Beausang: column 35, lines 31-39) during simulation of said circuit as a function of ones of said defined behavioral relationships (Dearth: column 1, lines 58-60).

Claim 2. The IC simulation system as set forth in Claim 1 comprising a processor (Dearth: column 7, line 18) and associated memory (Sharma: column 32, line 10).

Claim 3. The IC simulation system as set forth in Claim 2 wherein said associated memory (Sharma: column 32, line 10) is operable to store an IC-design process program and wherein said processor (Dearth: column 7, line 18) is operable to execute (Sharma: column 31, lines 7-10) said IC-design process program.

Claim 4. The IC simulation system as set forth in Claim 2 wherein said associated memory (Sharma: column 32, line 10) is operable to store said circuit netlist (Sharma: column 1, line 24) as a data structure (Sharma: column 3, line 5).

Claim 5. The IC simulation system as set forth in Claim 1 wherein said each one of said

plurality of HDL modules (Sharma: title) is parameterized (Sharma: title) and specifies a logical operation.

Claim 6. The IC simulation system as set forth in Claim 5 further operable to selectively match, with directed acyclic graphs ("DAGs"), (Sharma: column 11, line 16) a logical operation of said HDL description with a parameterized (Sharma: title) HDL module that is capable of performing said logical operation.

Claim 7. The IC simulation system as set forth in Claim 1 wherein said timing-violation controller operates to not ignore ones of said selected timing violations (Beausang: column 35, lines 31-39) sensed during simulation of said circuit as a function of ones of said defined behavioral relationships (Dearth: column 1, lines 58-60).

Claim 8. A method of operating an integrated circuit ("IC") simulation system comprising the steps of: storing a plurality of Hardware Description Language ("HDL") modules (Sharma: title) in memory (Sharma: column 32, line 10), each one of said plurality of HDL modules (Sharma: title) representative of a circuit element; receiving a HDL description of a circuit to be simulated (Sharma: column 1, line 19); synthesizing a circuit netlist (Sharma: column 1, line 24) as a function of said received HDL circuit description and ones of said plurality of HDL modules (Sharma: title), said circuit netlist (Sharma: column 1, line 24) defining behavioral relationships (Dearth: column 1, lines 58-60) among associated ones of said ones of said plurality of HDL modules (Sharma:

title); and associating a timing-violation controller with said circuit netlist (Sharma: column 1, line 24), said timing-violation controller to ignore selected timing violations (Beausang: column 35, lines 31-39) sensed during simulation of said circuit as a function of ones of said defined behavioral relationships (Dearth: column 1, lines 58-60).

Claim 9. The method of operating said IC simulation system as set forth in Claim 8 wherein said IC simulation system comprises a processor (Dearth: column 7, line 18) that is associated with said memory (Sharma: column 32, line 10).

Claim 10. The method of operating said IC simulation system as set forth in Claim 9 further comprising the steps of: storing an IC-design process program; and executing said IC-design process program with said processor (Dearth: column 7, line 18).

Claim 11. The method of operating said IC simulation system as set forth in Claim 9 further comprising the step of storing said circuit netlist (Sharma: column 1, line 24) as a data structure (Sharma: column 3, line 5).

Claim 12. The method of operating said IC simulation system as set forth in Claim 8 wherein said each one of said plurality of HDL modules (Sharma: title) is parameterized (Sharma: title) and specifies a logical operation.

Claim 13. The method of operating said IC simulation system as set forth in Claim 12 further comprising the step of selectively matching, with directed acyclic graphs ("DAGs"), a logical operation of said HDL description with a parameterized (Sharma: title) HDL module that is capable of performing said logical operation.

Claim 14. The method of operating said IC simulation system as set forth in Claim 8 further comprising the step of operating said timing-violation controller to not ignore ones of said selected timing violations sensed (Beausang: column 35, lines 31-39) during simulation of said circuit.

Claim 15. A computer readable memory (Sharma: column 32, line 10) that directs a computer to operate as an integrated circuit ("IC") simulation system, comprising: a plurality of Hardware Description Language ("HDL") modules (Sharma: title) stored (Sharma: column 30, line 67) in said computer readable memory (Sharma: column 32, line 10), each one of said plurality of HDL modules (Sharma: title) representative of a circuit element; a HDL description of a circuit to be simulated (Sharma: column 1, line 19) stored (Sharma: column 30, line 67) in said computer readable memory (Sharma: column 32, line 10), executable instructions stored (Sharma: column 30, line 67) in said computer readable memory (Sharma: column 32, line 10) to synthesize a circuit netlist (Sharma: column 1, line 24 and column 35, line 51) as a function of said HDL circuit description and ones of said plurality of HDL modules (Sharma: title), said circuit netlist (Sharma: column 1, line 24) defining behavioral relationships (Dearth: column 1, lines

58-60) among associated ones of said ones of said plurality of HDL modules (Sharma: title); and executable instructions stored (Sharma: column 30, line 67) in said computer readable memory (Sharma: column 32, line 10) to associate a timing-violation controller with said circuit netlist (Sharma: column 1, line 24), said timing-violation controller to ignore selected timing violations (Beausang: column 35, lines 31-39) sensed during simulation of said circuit as a function of ones of said defined behavioral relationships (Dearth: column 1, lines 58-60).

Claim 16. The computer readable memory (Sharma: column 32, line 10) as set forth in Claim 15 further comprising an IC-design process program stored (Sharma: column 30, line 67) in said computer readable memory (Sharma: column 32, line 10).

Claim 17. The computer readable memory (Sharma: column 32, line 10) as set forth in Claim 15 wherein said circuit netlist (Sharma: column 1, line 24) is stored (Sharma: column 30, line 67) in said computer readable memory (Sharma: column 32, line 10) as a data structure (Sharma: column 3, line 5).

Claim 18. The computer readable memory (Sharma: column 32, line 10) as set forth in Claim 15 wherein said each one of said plurality of HDL modules (Sharma: title) is parameterized (Sharma: title) and specifies a logical operation.

Claim 19. The computer readable memory (Sharma: column 32, line 10) as set forth in Claim 18 further comprising executable instructions stored (Sharma: column 30, line 67) in said computer readable memory (Sharma: column 32, line 10) to selectively match, with directed acyclic graphs ("DAGs"), (Sharma: column 11, line 16) a logical operation of said HDL description with a parameterized (Sharma: title) HDL module that is capable of performing said logical operation.

Claim 20. The computer readable memory (Sharma: column 32, line 10) as set forth in Claim 15 further comprising executable instructions stored (Sharma: column 30, line 67) in said computer readable memory (Sharma: column 32, line 10) to operate said timing-violation controller to not ignore ones of said selected timing violations (Beausang: column 35, lines 31-39) sensed during of said circuit.

Section II: Response to Applicant's Arguments (Non-Compliance)

5. The applicants are thanked for addressing these issue. The Office acknowledges the amendments to the specification, claims and drawings within the prosecution. With regard to the Oath/Declaration, the Office recognizes the oaths filed on 04/30/2002 and 10/26/2001; however, the Office cannot delete the oath dated 10/26/2001 since its part of the record but acknowledges the 10/26/2001 oath was in error. Prosecution continues with the proper oath that was filed on 04/30/2002. Furthermore, the 112 1st enablement rejection is withdrawn.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Paul Rodriguez 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

April 16, 2006

TS

Paul L. Rodriguez 4/17/06
Primary Examiner
Art Unit 2125